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RN-6787

B. E. - III (Sem. V) (EC/ECC) Examination

May / June – 2010

Microprocessor Programing & Interfacing

Time : **3** Hours] [Total Marks : **100**

Instructions :

(1)

નીચે દર્શાવેલ ☛ નિશાનીવાળી વિગતો ઉત્તરવહી પર અવશ્ય લખવી.
Fillup strictly the details of ☛ signs on your answer book.

Name of the Examination :

☛ B. E. - 3 (Sem. 5) (EC/ECC)

Name of the Subject :

☛ Microprocessor Programing & Interfacing

☛ Subject Code No. : 6 7 8 7 ☛ Section No. (1, 2,.....) : 1&2

Seat No. :

Student's Signature

(2) Attempt **all** questions.

(3) Figures to the right indicate full marks.

(4) Assume suitable data if necessary and mention clearly your assumptions.

(5) Use of scientific calculator Casio Fx-82, 83, 100 or equivalent of other make is allowed.

SECTION - I

1 (a) Answer the followings : **10**

(i) State the size of address bus and data bus in 8085 microprocessor.

(ii) State the functions of Ready and $\overline{\text{Reset in}}$ pins.

(iii) State the size of memory 6116 RAM and number of address lines required to interface this chip.

(iv) Write a control word for 8255 to program if in BSR made and set bits PC_7 and PC_3.

(v) What do you mean by key debouncing?

(b) With the neat diagram show the generation of control signals : $\overline{IOW}$, $\overline{IOR}$, $\overline{MEMR}$ and $\overline{MEMW}$ using 5

(i) 74138 decoder and

(ii) Logic gates

(c) With the neat diagram show the demultiplexing of $AD_0 - AD_7$ using 74373 latch. Explain the working. 5

2 (a) You are given 2732 EPROM chips how would you construct a 32kB EPROM board which can be interfaced with 8085. The starting address is 0000H. Show all necessary interfacing connections and memory map. Assume control signals are available. 8

(b) Design I/O mopped I/O interfacing to interfacing 8 switches using 74244 buffer and 8 common anode LEDs using 74373 latch. The address of input device is FOH and that of output device is F1H. Use absolute decoding and assume control signals are available. Write a program to read the position of switches. If the switch is closed make the LED of respective position ON and if the switch is open, make the respective LED OFF. 8

OR

2 (a) State four differences between memory mapped I/O and I/O mapped I.O. 4

(b) State differences between absolute and linear select (partial) decoding scheme. 4

(c) Draw and explain power ON reset circuit. 2

(d) Explain mode 0 operation of 8255. 5

3 Attempt any **three** : 15

(i) Interface DAC 0809 to 8085 microprocessor using 8255 and latch 74373. Assume suitable address and the latch is enabled by pin PBo of 8255 and PORT A is used to output data. Write a program to generate a saw-tooth signal using this scheme.

(ii) Explain mode 2 (Rate generator) and mode 3 (square wave generator) modes of 8254.

(iii) Deraw the internal block diagram of 8279 and explain its working.

(iv) Initialize 8254 such that it generates a –ve pulse of approximately 1 T-state after every 1 ms. Consider the crystal of 8085 to be 4 MHz and base address of 8254 is 10H.

(v) Draw a schematic to interface a 16 key matrix keyboard using PORT C of 8255. Write instrtuctions to initialize the port.

SECTION - II

4 (a) Answer the following : **10**

(i) Explain operation of instructions LXI H, 1000 H and DAA.

(ii) State function of PC and SP in 8085.

(iii) Which interrupt of 8085 has highest priority and which is non-maskable?

(iv) Identify addressing mode of instructions MVI A, OOH, SHLD 9000 H.

(v) State role of HOLD and HLDA pins in DMA data transfer.

(b) Draw and explain timing diagram of instruction IN 84H. **10**

5 (a) Draw the logic diagram of 8085 interrupt of structure. State vector locations of all interrupts. **7**

(b) Explain the role of priority encoder interrupt of with example. **8**

OR

5 (a) Draw and explain block diagram of 8259 programmable interrupt controller IC. **7**

(b) Write a short note on DMA and DMA controller IC 8257 interfacing. **8**

6 Attempt any **three** : **15**

(i) Write a program to count continuously in hexadecimal from FFH to OOH in a system with 0.5 μ s clock period. Use resister C to set up a 1 ms delay between each count and display the numbers at one of output ports.

(ii) A set of current reading is stored in memory locations starting at CO5OH. The end of the data string is indicated by the data byte OOH. Add the set of readings. The answer may be larger than FFH. Store answer in memory locations CO70H and CO71H.

(iii) Write a program to convert a BCD number to hex (binary) number. The BCD number is stored at COOOH and store hex number at COO1H location.

(iv) Write a main program to count continuously in binary with a one-second delay between each count. Write a service routine at CO70H to flash FFH five times when the program is interrupted with some appropriate relay between each flash.

(v) Write a program to set the zero flag and check whether the instruction JZ functions properly, without modifying the register contents other than flags.
